

LFTVS18-1F3

Low forward voltage Transil[™], transient voltage suppressor

Features

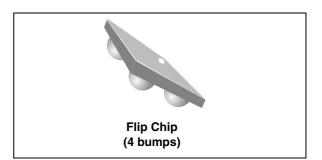
- Low forward voltage: 1.05 V @ 850 mA
- Peak pulse power (8/20 µs): 350 W
- Very low clamping factor V_{CL}/V_{BR}
- Unidirectional device
- Fast response time
- Very thin package: 0.605 mm
- RoHS compliant

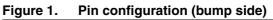
Complies with the following standards:

- IEC 61000-4-2 level 4
 - ± 15 kV (air discharge)
 - ±8 kV (contact discharge)

Description

The LFTVS18-1F3 is a single line diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD and EOS transient overvoltages.





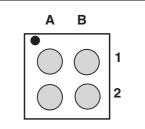
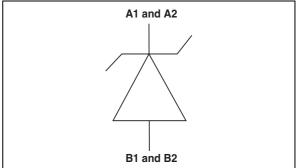


Figure 2. Device configuration



TM: Transil is a trademark of STMicroelectronics

1 Characteristics

	Absolute maximum rutings (ramb = 20 °C)			
Symbol	Parameter	Test condition	Value	Unit
D	Peak pulse power dissipation (10/1000 µs pulse)	T initial – T	44	w
P _{PP}	Peak pulse power dissipation (8/20 µs pulse)	T _j initial = T _{amb}	350	
I _{FSM}	Non repetitive surge peak forward current	t _p = 10 ms T _j initial = T _{amb}	11	A
Тj	Maximum operating junction temperature		125	°C
T _{stg}	Storage temperature range		-55 to +150	°C

Table 1. Absolute maximum ratings ($T_{amb} = 25 \ ^{\circ}C$)

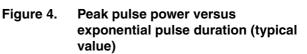
Table 2.	Electrical characteristics	$(T_{amb} = 25 \ ^{\circ}C)$
		(-amb) =

Symbol	Parameter		I.		
V _{BR}	Breakdown voltage		IF		
I _{RM}	Leakage current @ V _{RM}		IF		
V _{RM}	Stand-off voltage				
V _{CL}	Clamping voltage	VcL V	BR VRM	VF	5 W
R _d	Dynamic impedance			IRM	→ V
I _{PP}	Peak pulse current]			
αΤ	Voltage temperature coefficient		Slope = 1/Rd		
V _F	Forward voltage drop	↓		IPP	
Symbol	Test conditions	Min.	Тур.	Max.	Unit
V_{BR}	I _R = 1 mA	16		18	V
I _{RM}	V _{RM} = 10 V			500	nA
V _{CL}	$I_{PP} = 1 A^{(1)}$			19	V
V _F	I _F = 850 mA			1.05	V
αΤ				9	10 ⁻⁴ / °C
C _{line}	$V_R = 0 V, V_{OSC} = 30 mV, F = 1 MHz$		130		pF

1. 8 / 20 µs pulse waveform



Figure 3. Relative variation of peak pulse power versus initial junction temperature



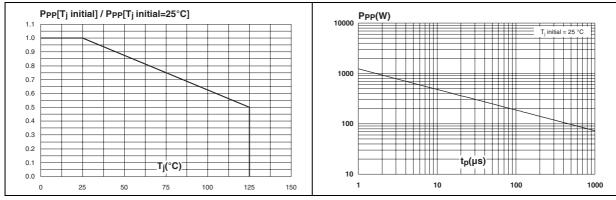
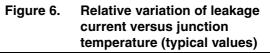


Figure 5. Clamping voltage versus peak pulse current (typical values)



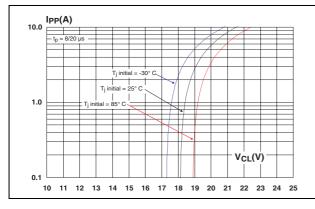


Figure 7. Forward voltage drop versus peak forward current (typical values)

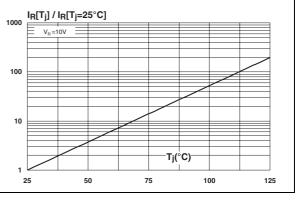
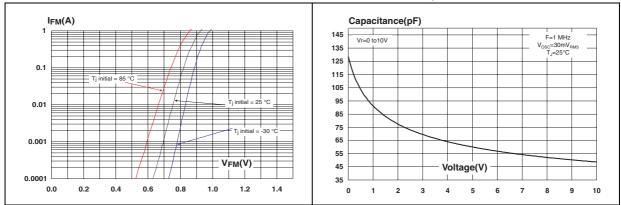


Figure 8. Junction capacitance versus reverse voltage applied (typical values)



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Figure 9. Breakdown voltage versus initial Figure 10. Frequency response junction temperature (typical value)

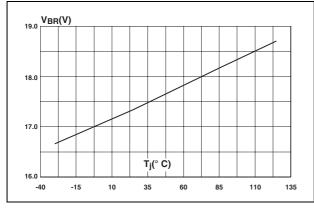


Figure 11. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

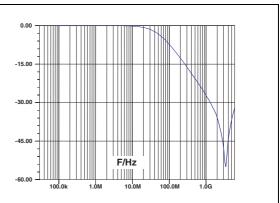
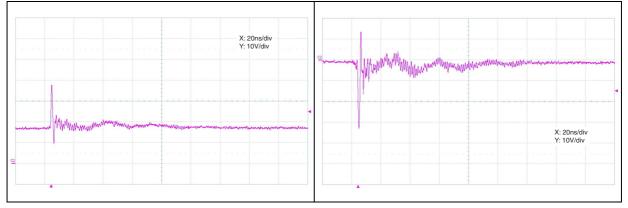
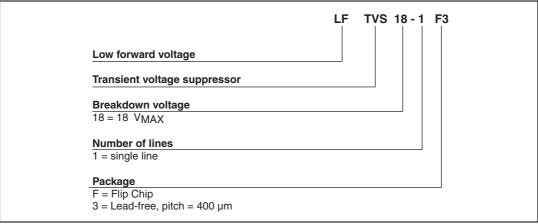


Figure 12. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



2 Ordering information scheme

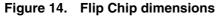
Figure 13. Ordering information scheme

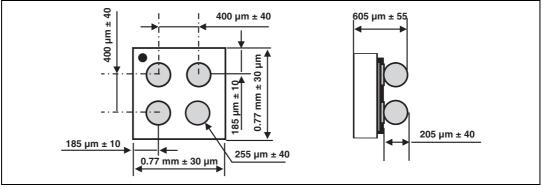




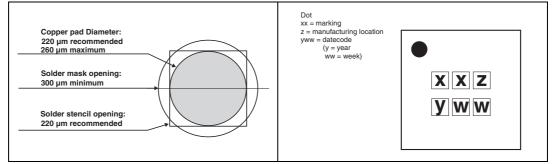
3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.











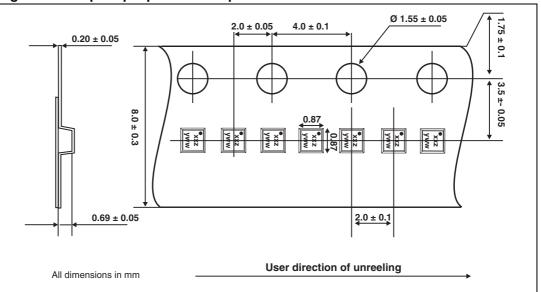


Figure 17. Flip Chip tape and reel specifications

Note: More information is available in the application notes: AN2348: "400 μm flip chip: Package description and recommendations for use" AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Table 3.	Ordering	information
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Order code	Marking	Package	Weight	Base qty	Delivery mode
LFTVS18-1F3	EM	Flip Chip	0.86 mg	10 000	Tape and reel (7")

5 Revision history

Table 4.Document revision history

Date	Revision	Changes
06-Mar-2008	1	Initial release.
04-Sep-2008	2	Updated V _F to 1.05 V. Updated <i>Figure 17</i> to show pitch of 2.0 mm. Updated I _{FSM} to 11 A. Updated <i>Figure 5</i> , <i>Figure 7</i> , and <i>Figure 8</i> .



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